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(71) Applicant: HARRIS CORPORATION
Melbourne, Florida 32903 (US)

(72) Inventors:
- Bagley, Patrick A.
West Melbourne, Florida 32904 (US)
- Rivoli, Anthony L.
Palm Bay, Florida 32905 (US)
- Young, William R.
Palm Bay, Florida 32907 (US)
- Delgado, Jose A.
Valkaria, Florida 32905 (US)
- Gaul, Stephen J.
Satellite Beach, Florida 32937 (US)

(74) Representative:
Fleuchaus, Leo, Dipl.-Ing. et al
Melchiorstrasse 42
81479 München (DE)

(54) **Integrated circuit air bridge structures and methods of fabricating same**

(57) Conductive elements may be incorporated in the devices at the integrated circuit level. An elongated conductor is formed over the dielectric layer and is encased in dielectric material. Then, portions of the substrate or the dielectric layer, or both, are removed to expose the encased elongated conductor to air. The method contemplates using sacrificial materials located between the encased conductor in the substrate. Removing the sacrificial material forms an air bridge cavity. The methods of the invention also include removing portions of the substrate in order to form the air bridge cavity. In a bonded substrate structure, a device substrate is bonded to a handle substrate, typically with an oxide bonding layer. Trench isolation is a common step used in the formation of devices and bonded substrates. The air bridge of the invention is compatible with the trench forming steps that are typically used in bonded substrates. In one bonded substrate embodiment, trenches are formed down to the oxide bonding layer. The trenches are coated with a dielectric, filled, and planarized. The dielectric layer covers the planarized trenches and elongated conductors are patterned on the dielectric layer over the air bridge trenches. Another dielectric layer covers the patterned conductors in order to encase them in a dielectric. Then the substrate is further patterned and etched to remove material from between the filled air bridge trenches. The final structure provides air bridge conductors encased in a dielectric that is spaced from the bonding oxide layer.

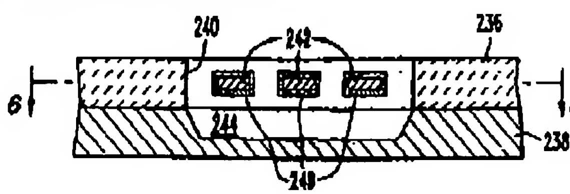

FIG. 5

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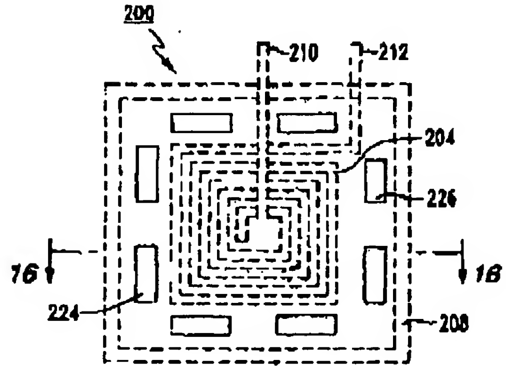

FIG. 17

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Description

The present invention relates to integrated circuit air bridge structures and methods of fabricating such structures which are hermetically sealed so as to protect the integrated circuits and any components, such as interconnecting conductors air bridges, inductors or capacitors, against damage or contamination from outside the device.

In order to reduce interconnect capacitances in high performance and high frequency processes, air bridges are often used. A typical air bridge is formed using a second layer of interconnect metal deposited and patterned over a sacrificial material. The sacrificial material is later removed to leave a metal lead surrounded by air rather than a dielectric, such as oxide. The capacitance to the substrate and to other metal lead is thus reduced since air has a lower dielectric constant than do solid insulators such as silicon dioxide or silicon nitride.

However, traditional air bridge manufacturing techniques and structures have several disadvantages. The length of an air bridge is often limited by flexure of metal between two vias. So, relatively long air bridges can only be manufactured by stitching together multiple lengths of short air bridges. Another problem is that circuits fabricated with air bridges cannot be passivated. In a normal process, a passivation layer is deposited on top of an integrated circuit. Typical passivation layers are silicon oxide or silicon nitride. However, for air bridge structures, the passivation layer has to be omitted otherwise the passivation layer will fill the air under the bridge and thereby increase the capacitance of the air bridge or damage the bridge itself.

Accordingly, there has arisen a need for air bridges that can be made of longer lengths of metal than are available in air bridges of the prior art and also for air bridges that can be incorporated into integrated circuits where such circuits have a passivation layer.

An object of the present invention is to provide improved integrated circuit air bridge structures which may be fabricated at the substrate level and which are passivated in the course of fabrication thereby avoiding the need for ceramic packaging or encapsulation, without materially increasing the volume occupied by the integrated circuit and any components, and to provide improved integrated circuit air bridge structures having air bridges or other components made out of conductive elements (e.g., inductors or capacitors), wherein sufficient spacing is provided between the air bridges of the components and the active integrated circuit so as to reduce the effect of parasitic capacitance between the conductive elements and the circuits and adversely affecting the high frequency response of these circuits.

An integrated circuit structure in accordance with the invention provides an air bridge fabricated on the same die as the integrated circuit to which the air bridge is connected. The invention provides an on-silicon air bridge that is compatible with single substrate and bonded substrate structures. The invention provides an air bridge structure on a semiconductor substrate or a device substrate. The device or semiconductor substrate may have one or more integrated circuits or semiconductor devices formed therein. The air bridge structure comprises an elongated metal conductor that is encased in a dielectric sheath. At least a portion of the sheath is exposed to ambient atmosphere. In one embodiment, the entire sheath is exposed to atmosphere. However, other embodiments expose a substantial portion of the sheath to ambient atmosphere in order to reduce the dielectric coupling between the sheath and the semiconductor substrate. In a typical construction, the encased conductor crosses a cavity in the substrate. The encased conductor is supported in its transit across the cavity by posts that extend from the lower surface of the cavity. The support posts comprise dielectric material, substrate material, or both.

The air bridge structure is made by forming a dielectric layer over semiconductor substrate. An elongated conductor is formed over the dielectric layer and is encased in dielectric material. Then, portions of the substrate or the dielectric layer, or both, are removed to expose the encased elongated conductor to air. The method contemplates using sacrificial materials located between the encased conductor in the substrate. Removing the sacrificial material forms an air bridge cavity. The methods of the invention also include removing portions of the substrate in order to form the air bridge cavity.

Particular embodiments of the invention include a cavity formed in the substrate and/or in the dielectric layer on the substrate. The encased conductors extend across the cavity and enter and exit the dielectric layer overlying the cavity.

In a bonded substrate structure, a device substrate is bonded to a handle substrate, typically with an oxide bonding layer. An air bridge structure is formed in the device substrate in several ways. Trench isolation is a common step used in the formation of devices and bonded substrates. The air bridge of the invention is compatible with the trench forming steps that are typically used in bonded substrates. In one bonded substrate embodiment, trenches are formed down to the oxide bonding layer. The trenches are coated with a dielectric, filled, and planarized. The dielectric layer covers the planarized trenches and elongated conductors are patterned on the dielectric layer over the air bridge trenches. Another dielectric layer covers the patterned conductors in order to encase them in a dielectric. Then the substrate is further patterned and etched to remove material from between the filled air bridge trenches. The final structure provides air bridge conductors encased in a dielectric that is spaced from the bonding oxide layer.

Bonded substrate structures are used to form inductors. In one embodiment, elongated conductors are encased in a dielectric layer that is disposed over a device substrate region located between isolating

trenches. Vias are opened in the dielectric layer and substrate material is removed to form an air bridge cavity beneath the encased conductors. Two air bridge cavities may be formed near one another and separated by a third cavity. Over each air bridge cavity conductors are patterned in a continuous, spiral path of metal in order to form an inductors. The third cavity is filled with ferromagnetic material.

Two further embodiments of the invention use a sacrificial layer for forming a cavity beneath an elongated, encased conductor. In one embodiment, a sacrificial layer of polysilicon is formed over a first dielectric layer that is on the semiconductor substrate. An encased conductor is formed over the sacrificial layer. Vias are opened to the sacrificial polysilicon and the polysilicon is removed to leave an air bridge cavity beneath the encased conductor and between the encased conductor and the silicon substrate. In an alternate embodiment, the dielectric layer on the surface of the substrate is partially removed before the sacrificial polysilicon is deposited. The sacrificial polysilicon is removed along with portions of the underlying substrate. The latter provides an enlarged air bridge cavity beneath the encased conductor.

The present invention includes an air bridge structure in a semiconductor substrate having one or more integrated circuits or semiconductor devices therein comprising an elongated metal conductor having a dielectric coating around at least a portion of the length of said conductor, said sheath being exposed to ambient atmosphere.

The invention also includes a method for forming an air bridge conductor comprising the steps of, depositing a dielectric layer over a semiconductor substrate, forming an elongated conductor over the substrate, encasing the elongated conductor in a dielectric sheath, and removing a portion of one or more layers proximate the sheathed conductor to form an air bridge conductor.

The invention will now be described by way of example with reference to the accompanying drawings in which

Figures 1-4 show the device illustrated in Figure 5 in successive stages of the fabrication thereof;

Figure 5 is a sectional view of a portion of an integrated circuit device having conductive members disposed in so-called "air bridge" configuration over an open space within the device;

Figure 6 is a fragmentary plan view illustrating the portion of the device shown in Figure 5; the view being taken along the line 6-6 in Figure 5;

Figures 7 and 8 illustrate a device similar to that shown in Figure 5;

Figures 9A-9C and 10A, 10B are fragmentary views, the view in Figures 9C being taken along the line 9C-9C in Figure 9B, the views illustrating means for support of conductive elements in the open space of an integrated circuit device;

Figures 11-15 show progressive steps in the formation of a bonded substrate with an air bridge formed in the device substrate;

Figure 16 is a fragmentary, sectional view of a portion of an enclosed, multi-layer integrated circuit device where a conductive member forming an inductor is located over an open space, all in accordance with still another embodiment of the invention, which provides contamination and damage protection and ease of handling during manufacture of integrated circuit devices, the view being taken along the line 16-16 in Figure 17;

Figure 17 is a plan view of the portion of the device shown in Figure 16;

Figures 18 to 20 are sectional views illustrating the device shown in Figures 16 and 17 in successive stages of the manufacture thereof;

Figure 21 is a sectional view of a device similar to that shown in Figure 16 wherein an internal core of ferromagnetic material is provided within the device;

Figures 22 and 23 are sectional views of the device shown in Figure 24 during an earlier and later stage in the fabrication thereof;

Figure 24 is a sectional view of a portion of an integrated circuit device of bonded layers including a conductive layer providing an interconnection suspended and bridging an open space in the device;

Figure 25 is a fragmentary plan view of the portion of the device shown in Figure 24;

Figure 26 is a sectional view of a portion of a bonded, enclosed, multi-layer device having a conductive layer which provides an interconnection over an open space in the device in accordance with another embodiment of the invention;

Figure 27 is a sectional view of the device shown in Figure 26 in a later stage of manufacture.

The air bridge structure shown in Figures 5 and 6 is made in accordance with the process steps shown in Figures 1-4. A suitable silicon substrate 238 has a layer of silicon dioxide 236 deposited or grown on one surface. That surface is processed to form the air bridge structure of Figures 5 and 6

By referring to Figures 1-4, the steps in the process of fabricating the devices of Figures 5 and 6 will become more apparent. First, trenches 220 are formed in an oxide layer 236 that covers substrate 238. The trenches 220 are coated with a layer of silicon nitride 247 or any other dielectric that can be selectively etched with respect to oxide layer 236. Next, a layer of metal 242 is deposited on the surface and in the trenches 220. The surface is then coated with a layer of photoresist 250. The photoresist and metal layer are planarized by a reactive ion etch that uses the nitride layer 247 as an etch stop. After the etch, the remaining photoresist is stripped and a second nitride layer is deposited to cover the metal in the trenches to form nitride sheaths 249 that surround the metal 242 in each trench. Another layer of photoresist 150 is deposited and patterned to

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protect the nitride layer 249. The exposed nitride on the surface is etched away leaving the sheath 249 around the conductors 242. The conductors 242 that remain may be partially imbedded in the insulative material layer 236 (the oxide) as shown in Figure. 4. As also shown in Figure. 4, the surface of the layer 236 may be masked with an etchant resistant mask 245 and then etched to form the cavity 240 and the cavity 244 as shown in Figure 5.

Referring to Figures 5 and 6 there is shown structure having a layer 236 of insulating material, such as oxide, and a substrate layer 238 of semiconductive material, such as silicon, in which integrated circuits may be formed. Supported in the layer 236 and bridging an opening 240 therein are a plurality of conductors 242 which define air bridges for interconnecting integrated circuits (not shown) in the silicon substrate 238. A cavity 244 in the substrate 238 is disposed in alignment with the opening 240. The opening and the cavity provide an air dielectric which reduces parasitic capacitance between the circuits in the silicon substrate 238 and the air bridge conductors 242. Sheaths 249 around the conductors 242 protect the conductors against contamination or damage by, for example, flakes of conductive material which may be formed during the processing of the substrate 238 to provide the integrated circuits therein.

Support posts 248 (Figure.7) may be provided in the opening 240 and underlie the sheathed conductors 242. The support posts 248 provide added support for the conductors 242. A support post 248 may be aligned with the sheathed conductors 242. An anisotropic etch will remove silicon from areas not covered by the sheathed conductors to provide the supports 248 shown in Figure. 7.

The support posts may also be formed only of the oxide layer 236. The posts are coated with a protective layer of nitride 258 as shown in Figure. 8.

Referring to Figure. 9A an aluminum conductor 250 rests on oxide support post 252. The post is passivated by depositing a sheath of nitride 258 or other passivating material, as shown in Figures 9B and 9C. The conductor may be passivated by oxidation to provide a layer 254 of aluminum oxide (Al_2O_3) as shown in Figure. 10A. The metal conductor 242 or aluminum conductor 250 may be also be passivated by a sheath of silicon oxide 251 (SiO_2) covered by a sheath of polysilicon 256 (Figure. 10B), thus providing a dual layer sheath.

Turning to Figures 11-15, there is shown another embodiment of the invention formed on a bonded substrate structure. In Figure 11 there is a handle substrate 100 that is oxide bonded via oxide layer 102 to the device substrate 110. In a following step (Figure 12), the device substrate 110 is patterned to form a series of trenches 101 to the surface of the bond oxide layer 102. Next, (Figure. 13) an oxide layer 104 is either thermally grown or deposited over the surface of the device substrate and the trenches 101. The trenches 101 are filled with polysilicon 105 and planarized. Another layer of dielectric material, e.g., silicon dioxide, is deposited. A layer of metal 109 is deposited and etched to form the conductors 106 over trenches 101. Another oxide layer 108 covers the metal. The strucutre of Figure. 14 is then masked and etched to provide the separated posts 116, 114, 112 of Figure. 15. The air between the separated posts reduces the capacitance between the conductors 106. So, the air bridge structure formed by the process of Figures 11 15 uses trench techniques compatible with customary bonded substrate processing. The air bridge structure is thus formed at the level of the device substrate 110 and is readily interconnected with circuits in the device substrate 110 by customary metallization and interconnect techniques.

Referring to Figures 16 and 17 there is shown a device substrate 200 which is bonded to a handle substrate 202 via oxide bond layer 216. In device substrate 200 integrated circuits (not shown) and air bridge structure are formed. The device substrate contains an inductor coil 204 suspended over the interfacing surfaces 207 of the device substrate 200 and handle substrate 202 and separated therefrom by a space or void 208 which may be void except for posts 209.

The coil 204 provides the inductor and may be of the square spiral shape shown in Figure 17. The center and end contacts 210 and 212 to the ends of the coil 204 do not appear in Figure 16. These contacts are of metal just like the coil turns and may extend along posts 209 to the active integrated circuits in the device substrate 200 in a manner similar to connections from the coils and the embodiments of the invention heretofore described.

The coil 204 is an air bridge conductive element. The bridge and support for the element 204 is provided by a layer of dielectric material 205 having an extent beyond the outer periphery of the conductors of the coil 204. This bridge is also supported on the posts 208.

Device substrate 200 has a bottom oxide layer 216. Oxide layer 216 bonds the device substrate 200 to the handle substrate 202. Another trench in a center post 208 may be filled with polysilicon in which case a pair of voids 208A and 208B may be formed in the substrate 200.

The device substrate 200 is fabricated in process steps shown in Figures 18, 19 and 20. A device substrate 200 has a silicon substrate 220 covered with a layer of oxide 206 or other suitable dielectric that encases conductor coil 204. The coil 204 may be provided in a trench and then covered so as to form the layer of dielectric, insulating material 205. As an alternative, the coil 204 may be formed by depositing a metal layer on a dielectric layer, patterning the metal layer, and depositing a further layer of dielectric on the patterned metal layer.

As shown in Figure 19 the device substrate is patterned to form trenches 106. The trenches are opened, coated with a thermal oxide 107 and filled with undoped polysilicon 108. The bond layer 216 joins the handle substrate 202 (not shown) to the device substrate 220.

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As shown in Figure 20 vias 224 and 226 are etched into the layer 205. The silicon of device substrate 220 is removed from the region between the trenches 106 by a selective etch to form the void 206.

Referring to Figure 21 there is shown a structure similar to that shown in Figure 16 and like parts are indicated with like referenced numerals. A cylindrical post 230 is provided by forming a via in the layer 205 and removing silicon in a region between the trenches 110, 112. The cavity between trenches 110 and 112 is filled with a ferromagnetic material such as iron. The ferromagnetic post 230 extends into the area of the inductor coil 204 and is electromagnetically coupled thereto so as to enhance and increase the inductance of the coil.

An in-silicon air bridge as shown in Figure 24 may be formed by the process steps shown in Figures 22 and 23. Referring to Figures 24 and 25, there is shown another integrated circuit structure 54 with an air bridge conductor 42. The air bridge 42 is formed on a single semiconductor (silicon) substrate layer 52 having an insulative (SiO_2) layer 60 thereon.

As shown in Figures 22 and 23, the active integrated circuits may be formed separately in the substrate 52 and have connections such as conductor 42 between devices of the integrated circuit. The silicon substrate 52 has an insulating layer 60, typically an oxide layer, either thermally grown or deposited. A sacrificial layer of polysilicon 68 or other material covers the insulating layer 60. The sacrificial layer 68 is patterned to the desired shape of an air bridge cavity and is covered with an oxide layer 64. A layer of metal 42 is deposited on oxide layer 64 and is patterned into the desired conFigureuration of the air bridge conductor. The patterned conductor 42 is covered with an insulating layer 44 of oxide or nitride.

As shown in Figure 23, vias 74 and 76 are opened to remove the sacrificial polysilicon layer 68. A cavity 66 is created by etching and removing the polysilicon 68. Further vias 70, 72 are provided to contact the airbridge metal 42 as shown in Figure 25.

Referring to Figure 27, there is shown a structure similar to that shown in Figure 24 and like parts are labeled with like referenced numerals. Again, a layer of sacrificial polysilicon or metal, which is shown at 68 in Figure 26, is used. First, the surface oxide layer 60 is patterned to remove a portion of oxide layer 60. A sacrificial polysilicon layer 68 is deposited over the exposed substrate. The polysilicon layer 68 is covered with an oxide layer 64. the air bridge metal 42 is deposited on the oxide layer 64 patterned and covered with another oxide layer 44. Etch windows 74 and 76 provide etch holes for an etchant, for example, KOH, which etches the polysilicon metal 68 isotropically, but etches the silicon in the substrate 52 anisotropically thereby producing a deep cavity 66A. The anisotropic etching process to produce the deep void or cavity 66A may be carried out in accordance with the etch/removal method described in an article by Sugiyama, et al., entitled "Micro-diaphragm Pressure Sensor," IEDM 1986, pages 184-187. The void space 66A is aligned with the conductive element of the air bridge structure 42 and is operative to reduce parasitic capacitances in the device. Removing silicon not only reduces capacitance but also reduces parasitic image current induced in the silicon by currents flowing in a conductor above the silicon. Such induced current is reduced by the voids that space the conductors from the silicon. The devices are fabricated at the substrate level and then separated into dice having one or more active integrated circuits using scribes or trenches of the type conventionally used for die separation.

Conductive elements may be incorporated in the devices at the integrated circuit leve. An elongated conductor is formed over the dielectric layer and is encased in dielectric material. Then, portions of the substrate or the dielectric layer, or both, are removed to expose the encased elongated conductor to air. The method contemplates using sacrificial materials located between the encased conductor in the substrate. Removing the sacrificial material forms an air bridge cavity. The methods of the invention also include removing portions of the substrate in order to form the air bridge cavity. In a bonded substrate structure, a device substrate is bonded to a handle substrate, typically with an oxide bonding layer. Trench isolation is a common step used in the formation of devices and bonded substrates. The air bridge of the invention is compatible with the trench forming steps that are typically used in bonded substrates. In one bonded substrate embodiment, trenches are formed down to the oxide bonding layer. The trenches are coated with a dielectric, filled, and planarized. The dielectric layer covers the planarized trenches and elongated conductors are patterned on the dielectric layer over the air bridge trenches. Another dielectric layer covers the patterned conductors in order to encase them in a dielectric. Then the substrate is further patterned and etched to remove material from between the filled air bridge trenches. The final structure provides air bridge conductors encased in a dielectric that is spaced from the bonding oxide layer.

Claims

1. An air bridge structure in a semiconductor substrate having one or more integrated circuits or semiconductor devices therein comprising an elongated metal conductor having a dielectric coating around at least a portion of the length of said conductor, said sheath being exposed to ambient atmosphere.

2. An air bridge structure as claimed in claim 1 wherein the dielectric coating comprises a dielectric selected from the group consisting of silicon dioxide, silicon nitride, and aluminum oxide, and the conductor comprises aluminum.

3. An air abridge structure as claimed in claims 1 or 2,

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characterized by a support extending from a surface of the semiconductor substrate to the outer surface of the sheath for supporting the conductor.

4. An air bridge structure as claimed in claim 3 wherein the support comprises semiconductor material.

5. An air bridge structure as claimed in any one of claims 1 to 4 wherein a majority of the entire outer surface area of a portion of the sheath is exposed to ambient atmosphere.

6. An air bridge structure as claimed in claim 5 wherein the conductor is disposed opposite a cavity in the semiconductor substrate.

7. An air bridge as claimed in claim 6 wherein said conductor is formed into a spiral of adjacent turns to create an inductor, and the dielectric coating comprises a dielectric layer and an inductor is formed in the dielectric layer over a cavity in the semiconductor substrate.

8. An air bridge as claimed in claim 7 characterized in that at least a second inductor spaced from the first inductor by a core cavity, said core cavity is filled with ferromagnetic material.

9. An air bridge structure comprising:

a bonded substrate structure comprising a device substrate having an upper and lower surface with one or more semiconductor devices or integrated circuits formed in said device substrate, a handle substrate, and a bonding layer for bonding the lower surface of the device substrate to the handle substrate;
a cavity in said device substrate extending from the upper surface of the device substrate to the bonding layer
a post comprising an elongated strip of dielectric material extending from the bonding layer to about the upper surface of the device substrate;
a conductor encased in said elongated strip.

10. An air bridge structure as claimed in claim 9 wherein the post further comprises an elongated region of polysilicon disposed between the conductor and the bonding layer.

11. A method for forming an air bridge conductor comprising the steps of:

depositing a dielectric layer over a semiconductor substrate;

forming an elongated conductor over the substrate;

encasing the elongated conductor in a dielectric sheath;

removing a portion of one or more layers proximate the sheathed conductor to form an air bridge conductor.

12. A method as claimed in claim 11 wherein the portions removed comprise portions of the first dielectric layer, and additional portions removed comprises portions of the semiconductor substrate.

13. A method as claimed in claims 11 or 12 characterized by the step of depositing a sacrificial layer between the encased conductor and the semiconductor substrate and removing a portion of the sacrificial layer to form an air bridge cavity.

14. A method for forming an air bridge comprising the steps of:

bonding a device substrate to a handle substrate using an oxide bonding layer;
forming a plurality of trenches in the device substrate and extending to the oxide bonding layer;
coating the trenches with a first dielectric layer;
filling and planarizing the trenches to the level of the device substrate;
depositing a second dielectric layer over the planarized device substrate;
depositing a metal layer on the second dielectric layer;
patterning the metal layer to form conductors over the filled trenches;
covering the conductors with a third layer of dielectric;
selectively removing the dielectric material and the device substrate material from regions between the filled trenches to form air bridge conductors spaced from the bonding layer, encased in dielectric and laterally separated by ambient atmosphere.

15. A method as claimed in claim 14 characterized by the step of filling the coated trenches with polysilicon before planarizing.

16. A method as claimed in claims 14 or 15 characterized by forming first and second air bridge cavities with a single conductors extending in a spiral path across each cavity and encased in dielectric;

forming a third cavity between the first and second air bridge cavities;
filling the third cavity with ferromagnetic material.

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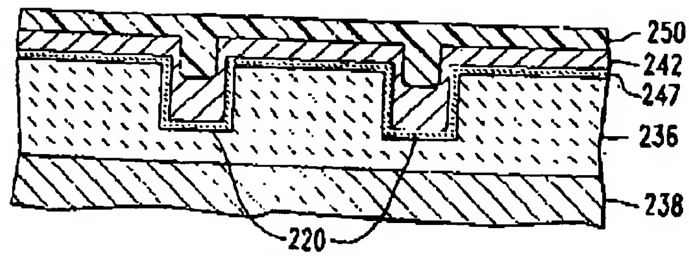

FIG. 1

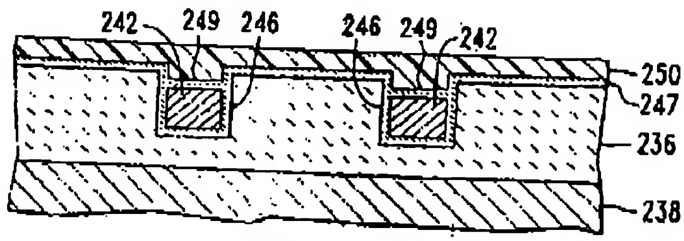

FIG. 2

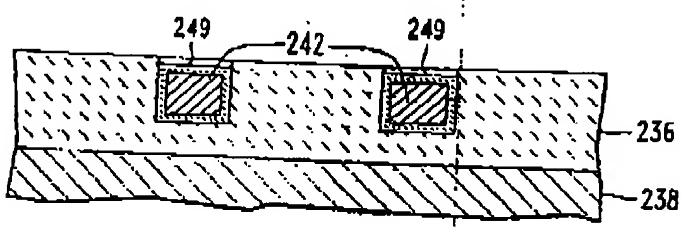

FIG. 3

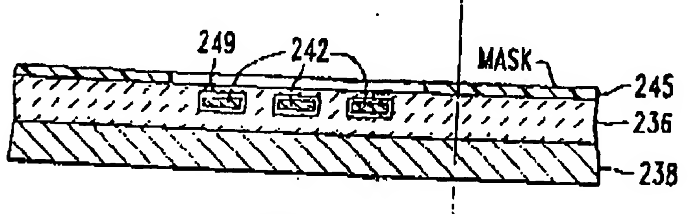

FIG. 4

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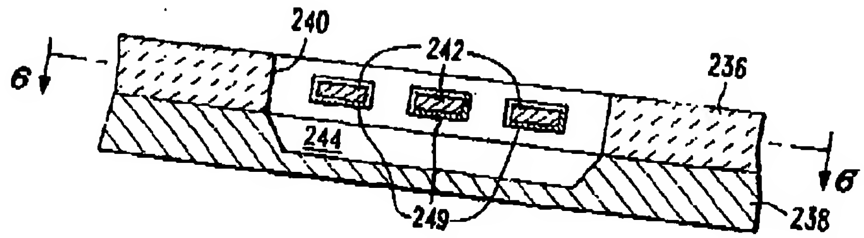

FIG. 5

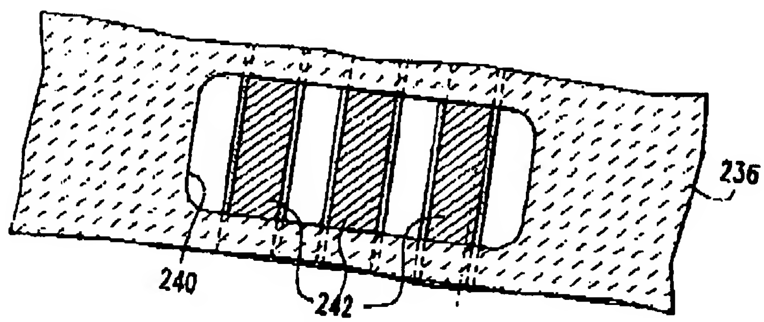

FIG. 6

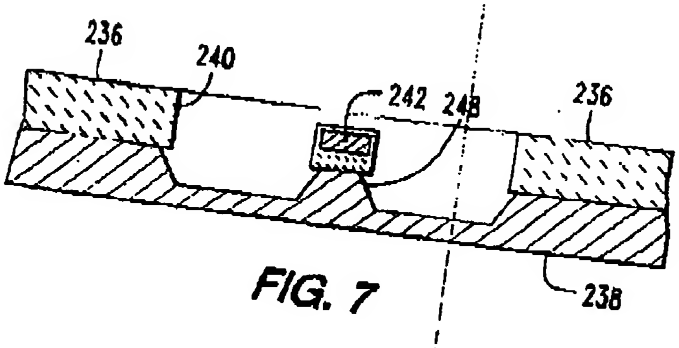

FIG. 7

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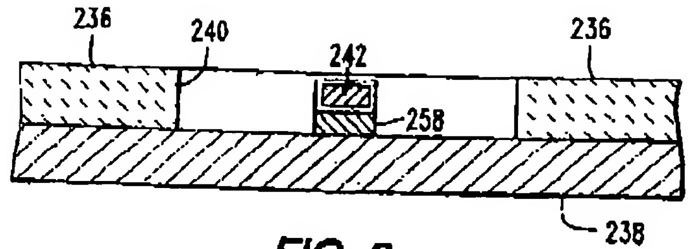

FIG. 8

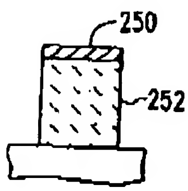

FIG. 9A

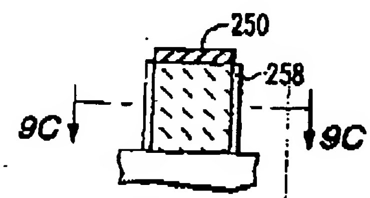

FIG. 9B

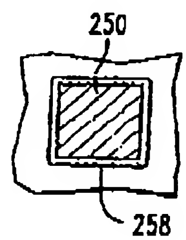

FIG. 9C

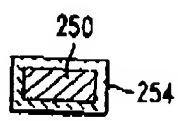

FIG. 10A

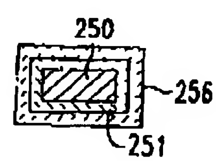

FIG. 10B

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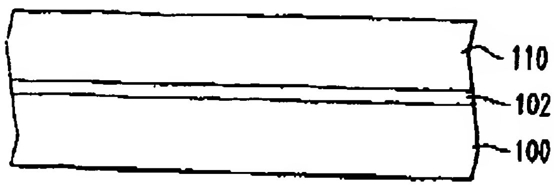

FIG. 11

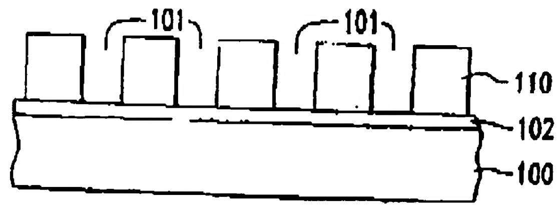

FIG. 12

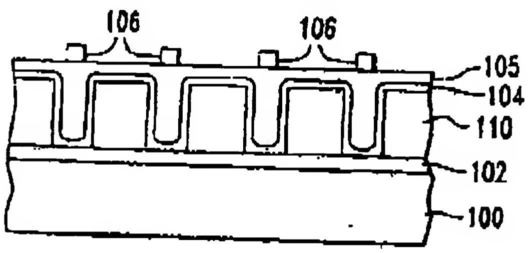

FIG. 13

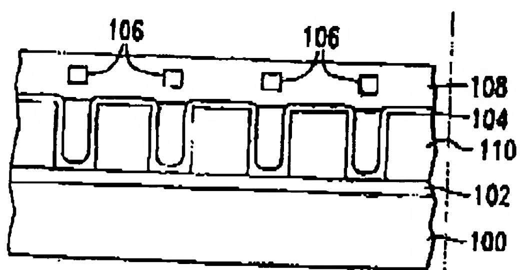

FIG. 14

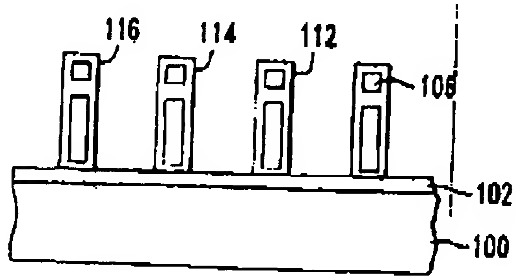

FIG. 15

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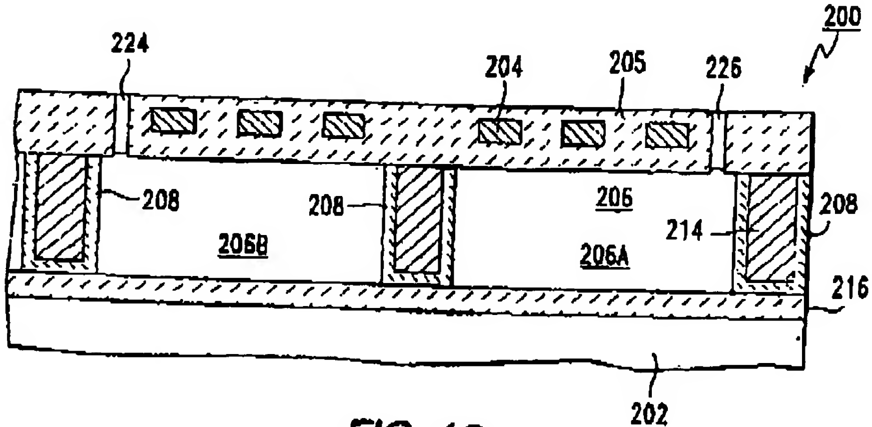

FIG. 16

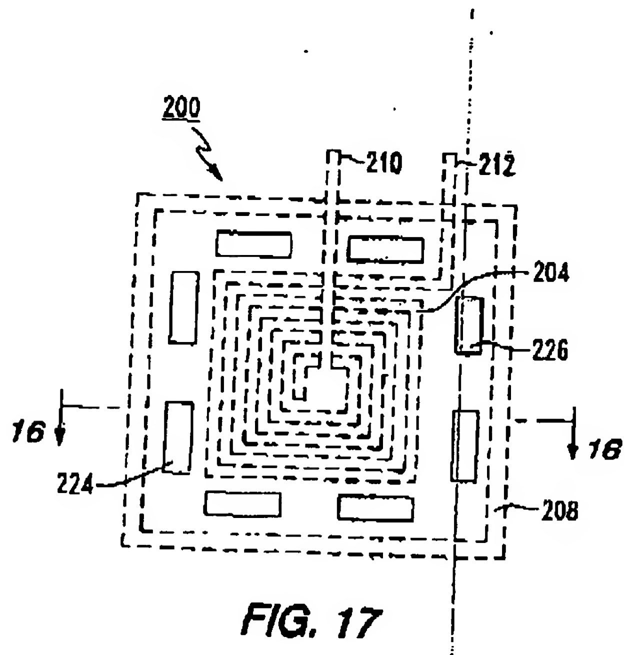

FIG. 17

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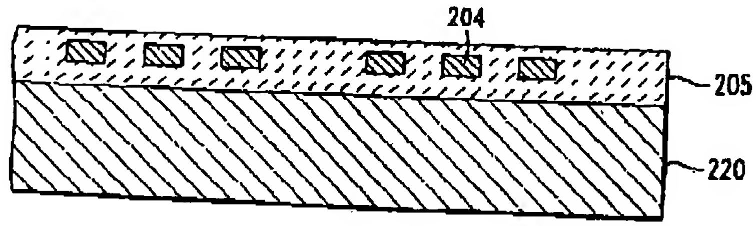

FIG. 18

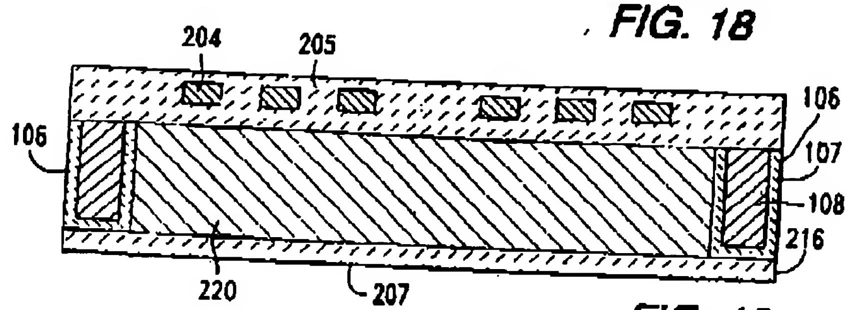

FIG. 19

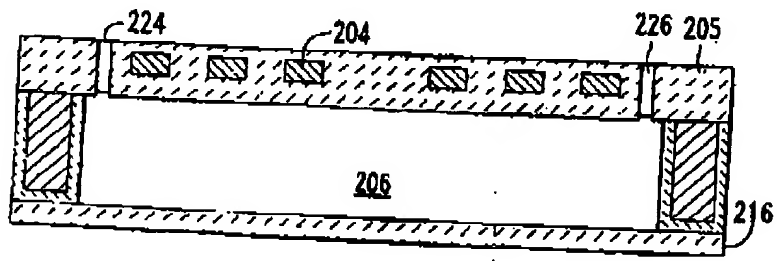

FIG. 20

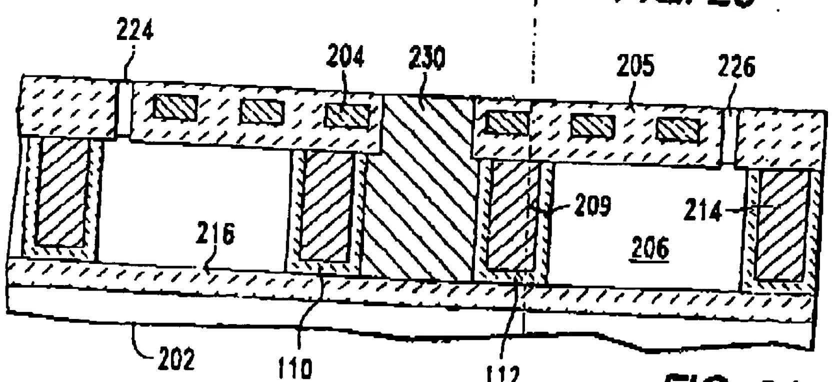

FIG. 21

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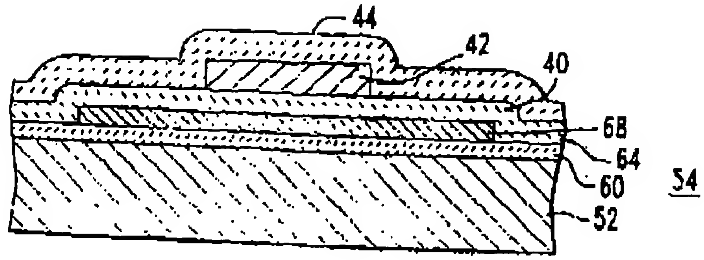

FIG. 22

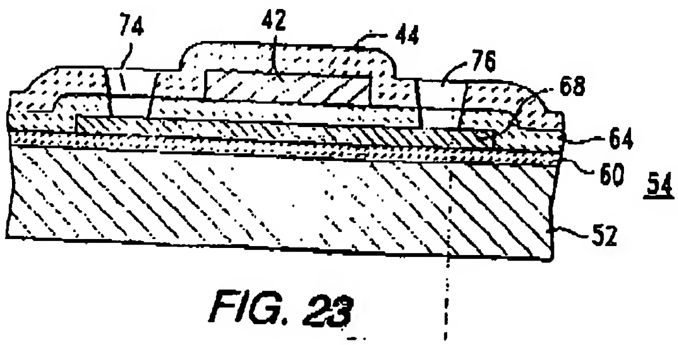

FIG. 23

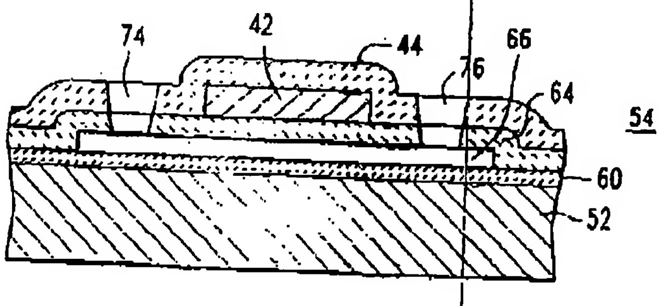

FIG. 24

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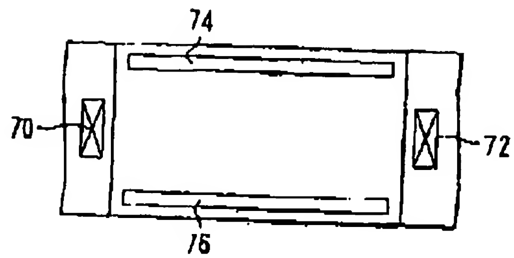

FIG. 25

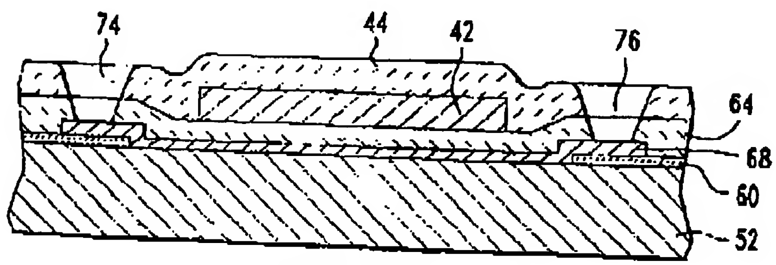

FIG. 26

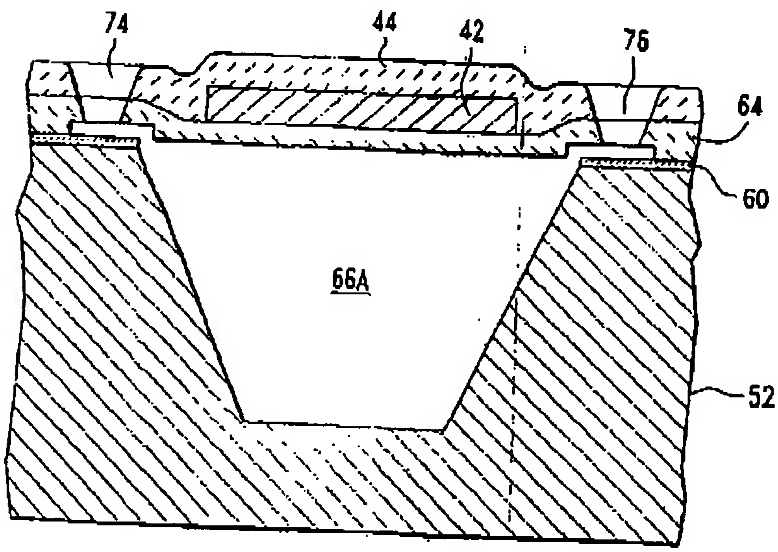

FIG. 27

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 10 0480

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y A	WO 94 17558 A (UNIV CALIFORNIA) 4 August 1994 * page 9, line 1 - page 11, line 10; figures 1,2,6A-8 *	1,2,5-7 3,4 9,11,12,14	H01L23/522 H01L21/768 H01L21/3205
Y A	EP 0 043 014 A (ROCKWELL INTERNATIONAL CORP) 6 January 1982 * page 4, line 26 - page 5, line 21; figures 6-9 *	3,4 9	
X Y A	EP 0 076 935 A (HONEYWELL INC) 20 April 1983 * page 5, line 15 - page 7, line 5; figures 1,3,4 * * page 32, line 11 - page 35, line 18 *	1,2,5,6,11,12 13 9,14	
D,Y	IEDM, 1986, pages 184-187, XP002039418 S. SUGIYAMA ET AL.: "Micro-diaphragm Pressure Sensor" * page 184, column 2, line 37 - page 185, line 32; figure 3 *	13	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	EP 0 523 450 A (SUMITOMO ELECTRIC INDUSTRIES) 20 January 1993 * page 3, column 3, line 25 - line 46; figure 1 *	7,8,16	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	1 September 1997	Albrecht, C

CATEGORY OF CITED DOCUMENTS

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